

DATA SHEET

PDTA123J series

PNP resistor-equipped transistors;

R1 = 2.2 k Ω , R2 = 47 k Ω

Product specification
Supersedes data of 2003 Apr 14

2004 Aug 02

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FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	–50	V
I _O	output current (DC)	–	–100	mA
R1	bias resistor	2.2	–	k Ω
R2	bias resistor	47	–	k Ω

DESCRIPTION

PNP resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN COMPLEMENT
	PHILIPS	EIAJ		
PDTA123JE	SOT416	SC-75	27	PDTC123JE
PDTA123JEF	SOT490	SC-89	27	PDTC123JEF
PDTA123JK	SOT346	SC-59	43	PDTC123JK
PDTA123JM	SOT883	SC-101	DG	PDTC123JM
PDTA123JS	SOT54 (TO-92)	SC-43	TA123J	PDTC123JS
PDTA123JT	SOT23	–	*23 ⁽¹⁾	PDTC123JT
PDTA123JU	SOT323	SC-70	*43 ⁽¹⁾	PDTC123JU

Note

- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTA123JS		1 2 3	base collector emitter
PDTA123JE PDTA123JEF PDTA123JK PDTA123JT PDTA123JU		1 2 3	base emitter collector
PDTA123JM		1 2 3	base emitter collector

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	–50	V
V _{CEO}	collector-emitter voltage	open base	–	–50	V
V _{EBO}	emitter-base voltage	open collector	–	–10	V
V _I	input voltage positive negative		–	+5	V
			–	–12	V
I _O	output current (DC)		–	–100	mA
I _{CM}	peak collector current		–	–100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT54	note 1	–	500	mW
	SOT23	note 1	–	250	mW
	SOT346	note 1	–	250	mW
	SOT323	note 1	–	200	mW
	SOT416	note 1	–	150	mW
	SOT490	notes 1 and 2	–	250	mW
SOT883	notes 2 and 3	–	250	mW	
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	in free air		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT416	note 1	833	K/W
	SOT490	notes 1 and 2	500	K/W
SOT883	notes 2 and 3	500	K/W	

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

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CHARACTERISTICS

$T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{\text{CB}} = -50 \text{ V}$; $I_{\text{E}} = 0$	–	–	–100	nA
I_{CEO}	collector-emitter cut-off current	$V_{\text{CE}} = -30 \text{ V}$; $I_{\text{B}} = 0$	–	–	–1	μA
		$V_{\text{CE}} = -30 \text{ V}$; $I_{\text{B}} = 0$; $T_{\text{j}} = 150 \text{ }^\circ\text{C}$	–	–	–50	μA
I_{EBO}	emitter-base cut-off current	$V_{\text{EB}} = -5 \text{ V}$; $I_{\text{C}} = 0$	–	–	–180	μA
h_{FE}	DC current gain	$V_{\text{CE}} = -5 \text{ V}$; $I_{\text{C}} = -10 \text{ mA}$	100	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_{\text{C}} = -5 \text{ mA}$; $I_{\text{B}} = -0.25 \text{ mA}$	–	–	–100	mV
$V_{\text{i(off)}}$	input-off voltage	$I_{\text{C}} = -100 \text{ }\mu\text{A}$; $V_{\text{CE}} = -5 \text{ V}$	–	–0.6	–0.5	V
$V_{\text{i(on)}}$	input-on voltage	$I_{\text{C}} = -5 \text{ mA}$; $V_{\text{CE}} = -0.3 \text{ V}$	–1.1	–0.75	–	V
R1	input resistor		1.54	2.2	2.86	$\text{k}\Omega$
$\frac{R2}{R1}$	resistor ratio		17	21	26	
C_{c}	collector capacitance	$I_{\text{E}} = i_{\text{e}} = 0$; $V_{\text{CB}} = -10 \text{ V}$; $f = 1 \text{ MHz}$	–	–	3	pF

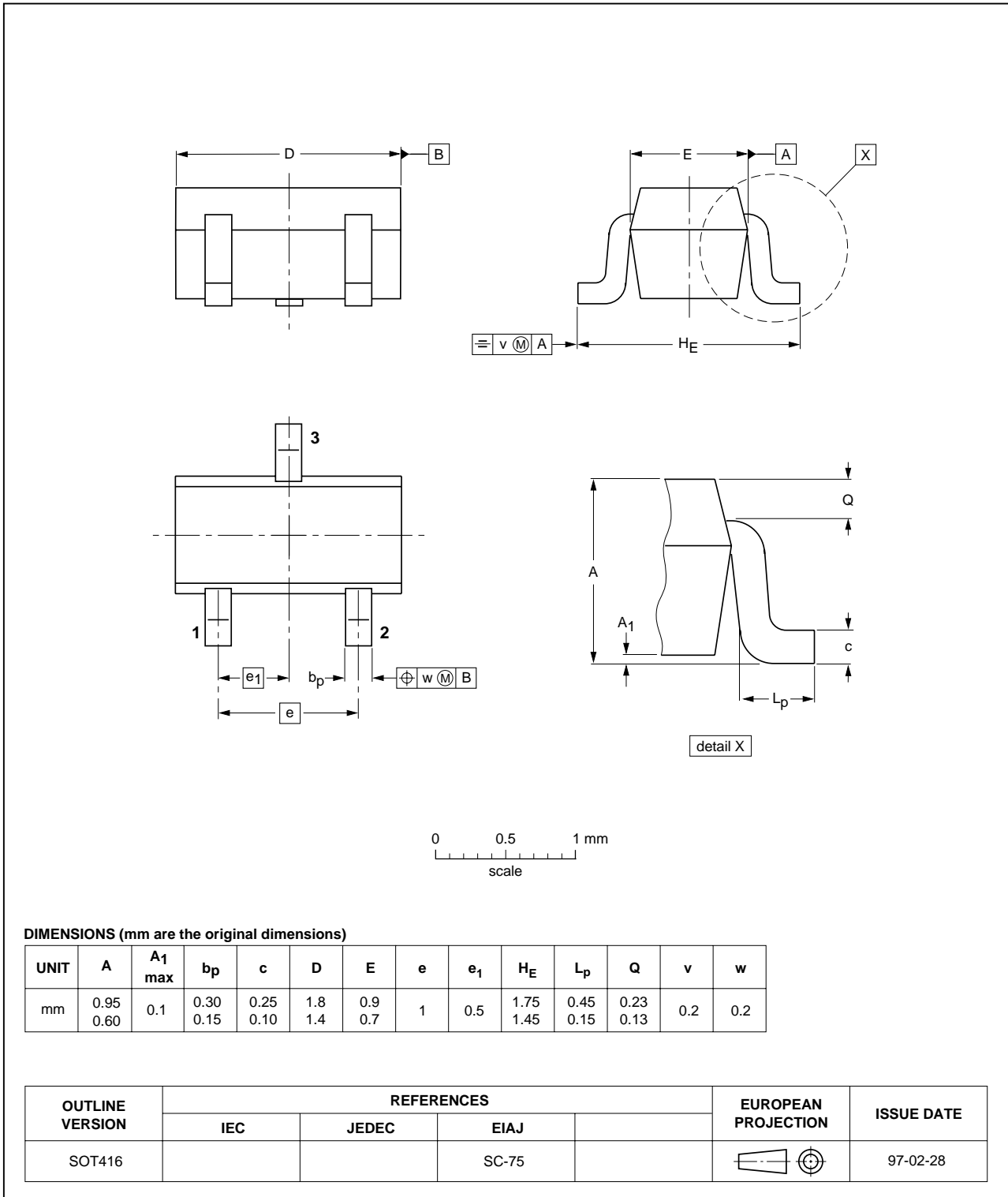
PNP resistor-equipped transistors;
R1 = 2.2 kΩ, R2 = 47 kΩ

PDTA123J series

PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT416

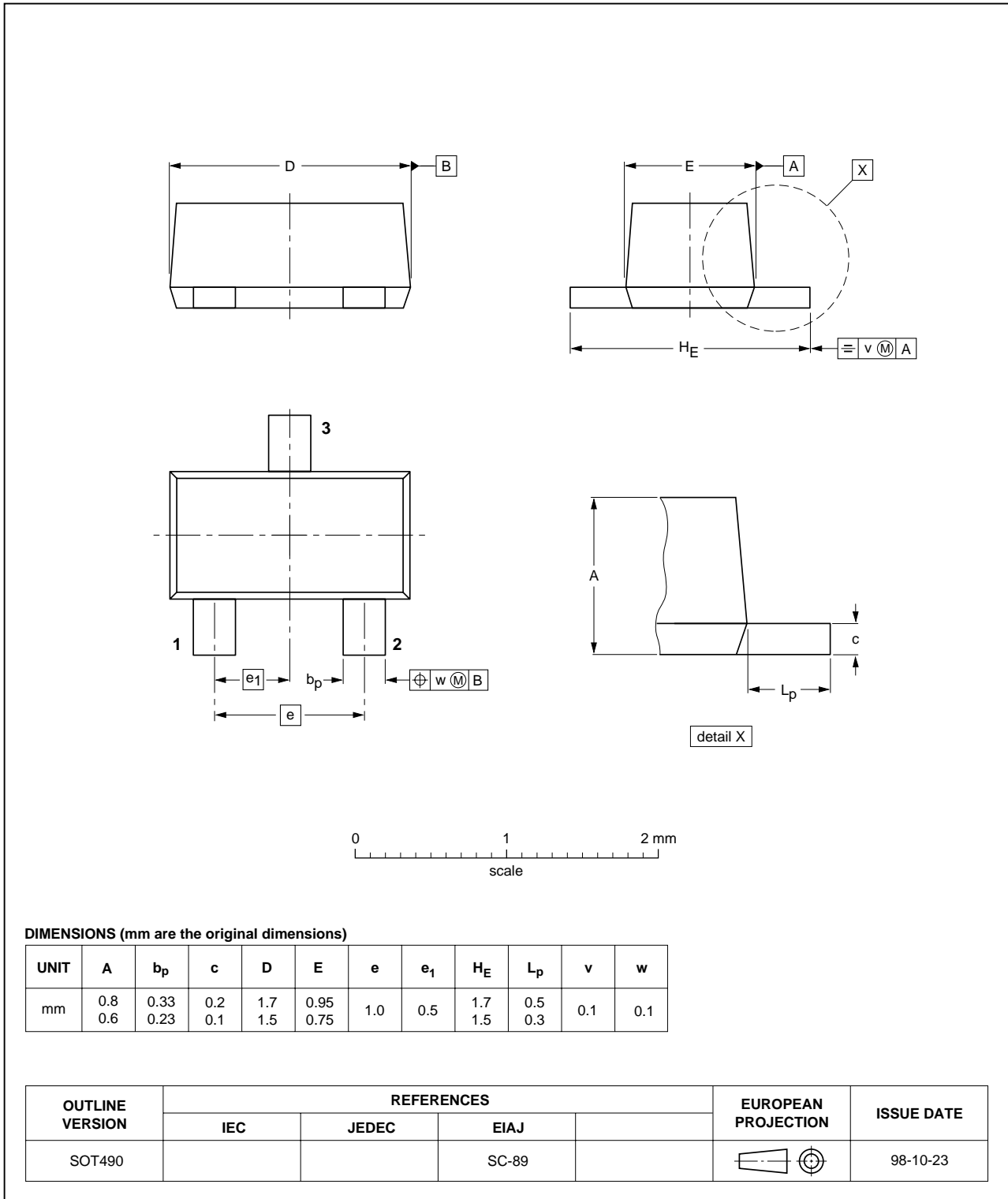


PNP resistor-equipped transistors;
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Plastic surface mounted package; 3 leads

SOT490



PNP resistor-equipped transistors;
R1 = 2.2 kΩ, R2 = 47 kΩ

PDTA123J series

Plastic surface mounted package; 3 leads

SOT346

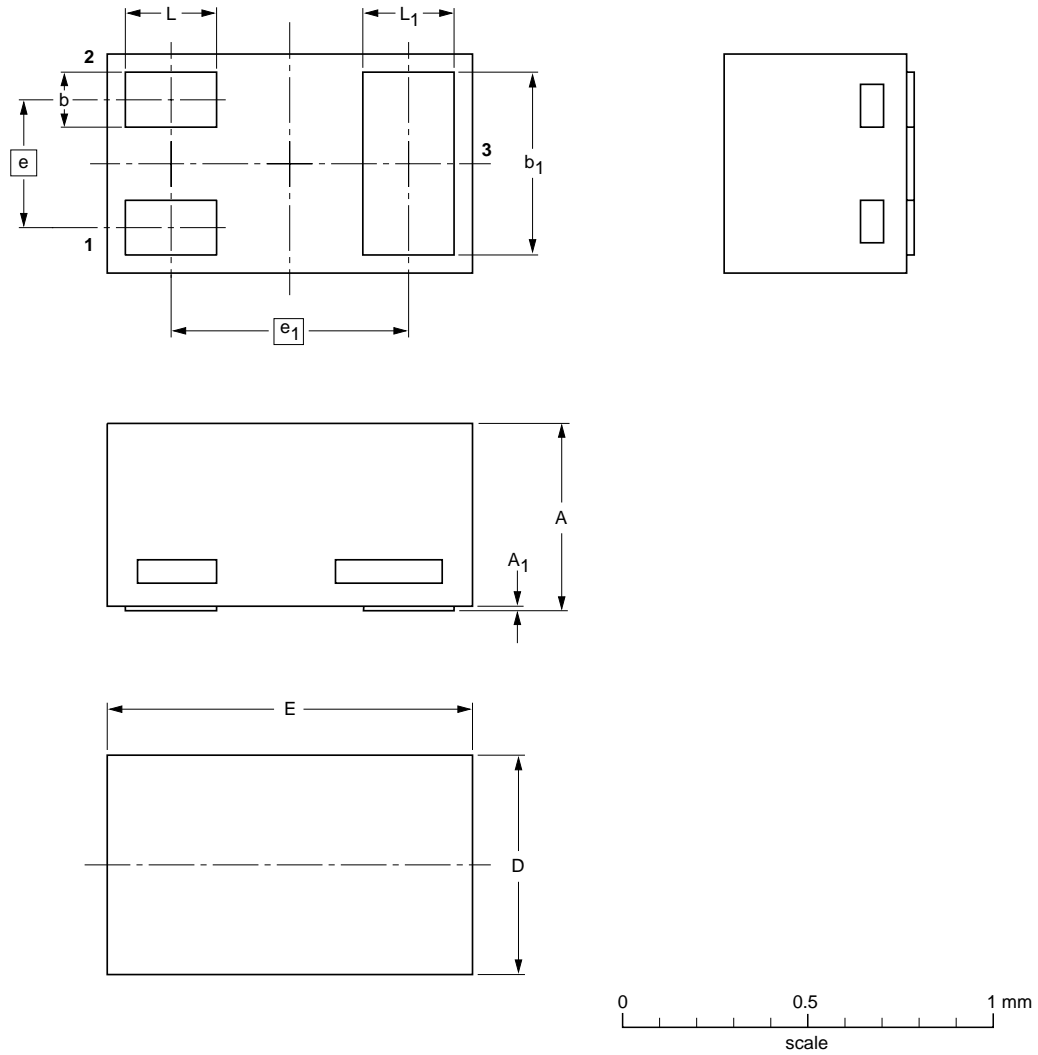


PNP resistor-equipped transistors;
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Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾	A ₁ max.	b	b ₁	D	E	e	e ₁	L	L ₁
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note

1. Including plating thickness

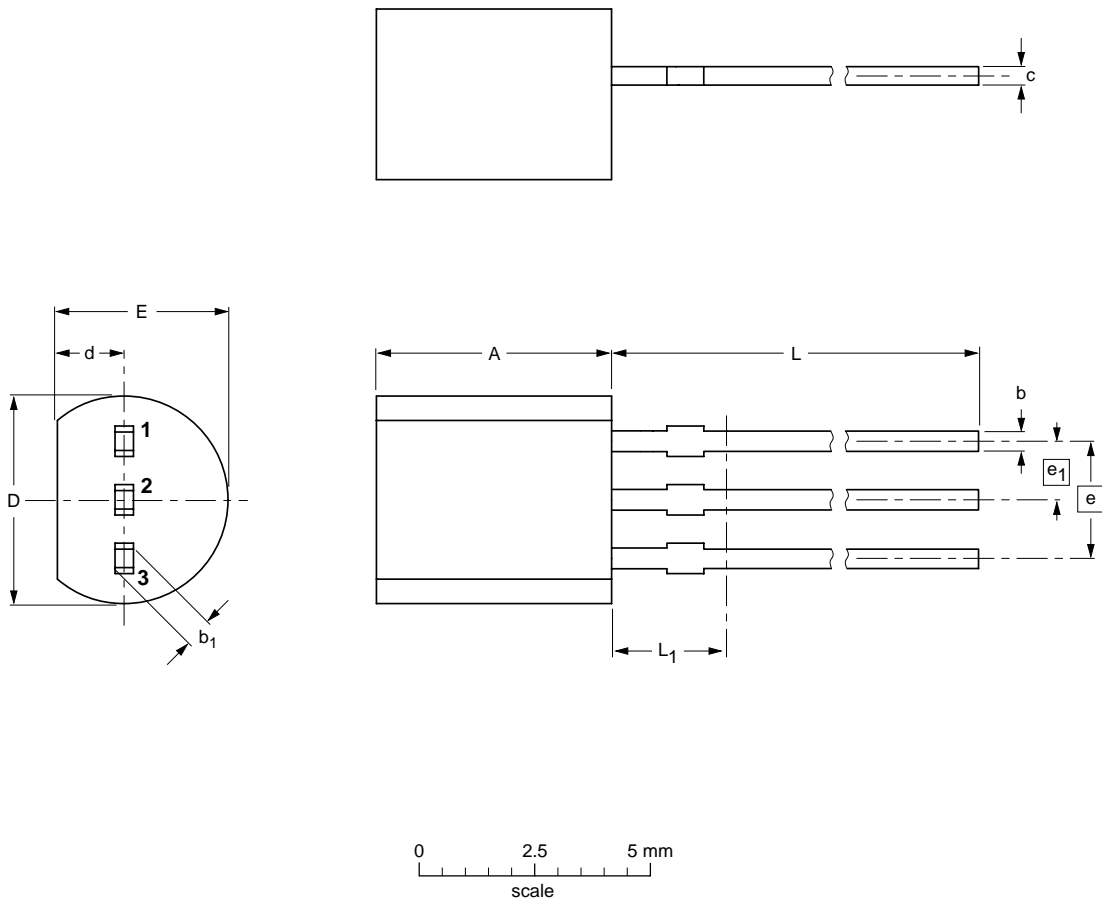
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT883			SC-101		03-02-05 03-04-03

PNP resistor-equipped transistors;
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PDTA123J series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		-97-02-28 04-06-28

PNP resistor-equipped transistors;
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Plastic surface mounted package; 3 leads

SOT23

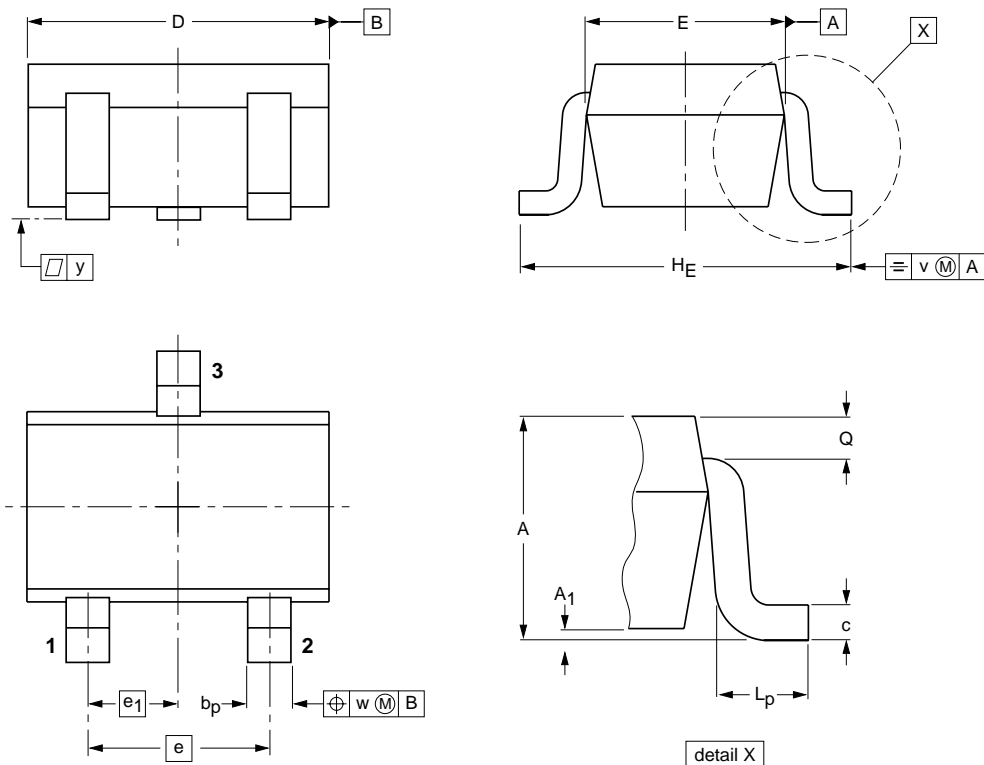


PNP resistor-equipped transistors;
R1 = 2.2 kΩ, R2 = 47 kΩ

PDTA123J series

Plastic surface mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

PNP resistor-equipped transistors;
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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Printed in The Netherlands

R75/04/pp14

Date of release: 2004 Aug 02

Document order number: 9397 750 13651

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